FIG. 1

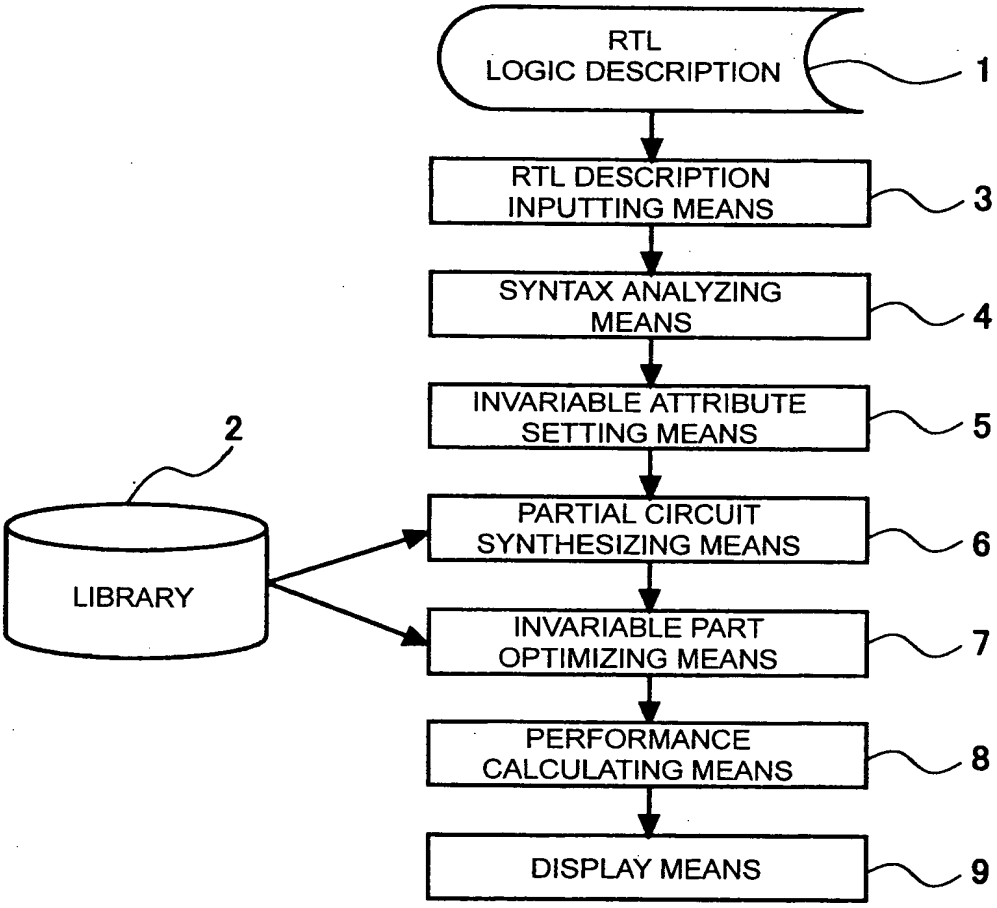
RTL
LOGIC DESCRIPTION
1
RTL DESCRIPTION
INPUTTING MEANS
3
SYNTAX ANALYZING
MEANS
4
INVARIABLE ATTRIBUTE
SETTING MEANS
5
2
PARTIAL CIRCUIT
SYNTHESIZING MEANS
6
LIBRARY
INVARIABLE PART
OPTIMIZING MEANS
7
PERFORMANCE
CALCULATING MEANS
8
DISPLAY MEANS
9

FIG. 2A

```
wire [7:0] A,B,Y;
wire sel;
...
assign Y = (sel==1'b1)?A+B:A;
```

FIG. 2B

signal	file	line
A[7:0]	design1.v	50
B[7:0]	design1.v	60
Y[7:0]	design1.v	70
sel	design1.v	65

FIG. 2C

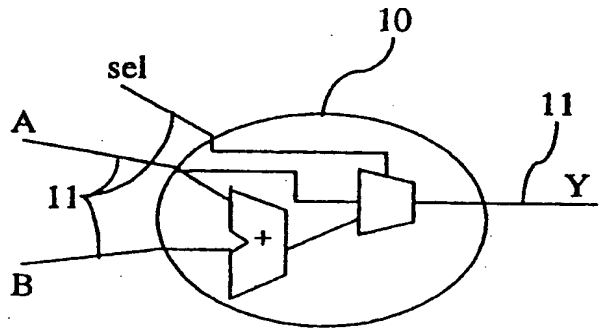

FIG. 3

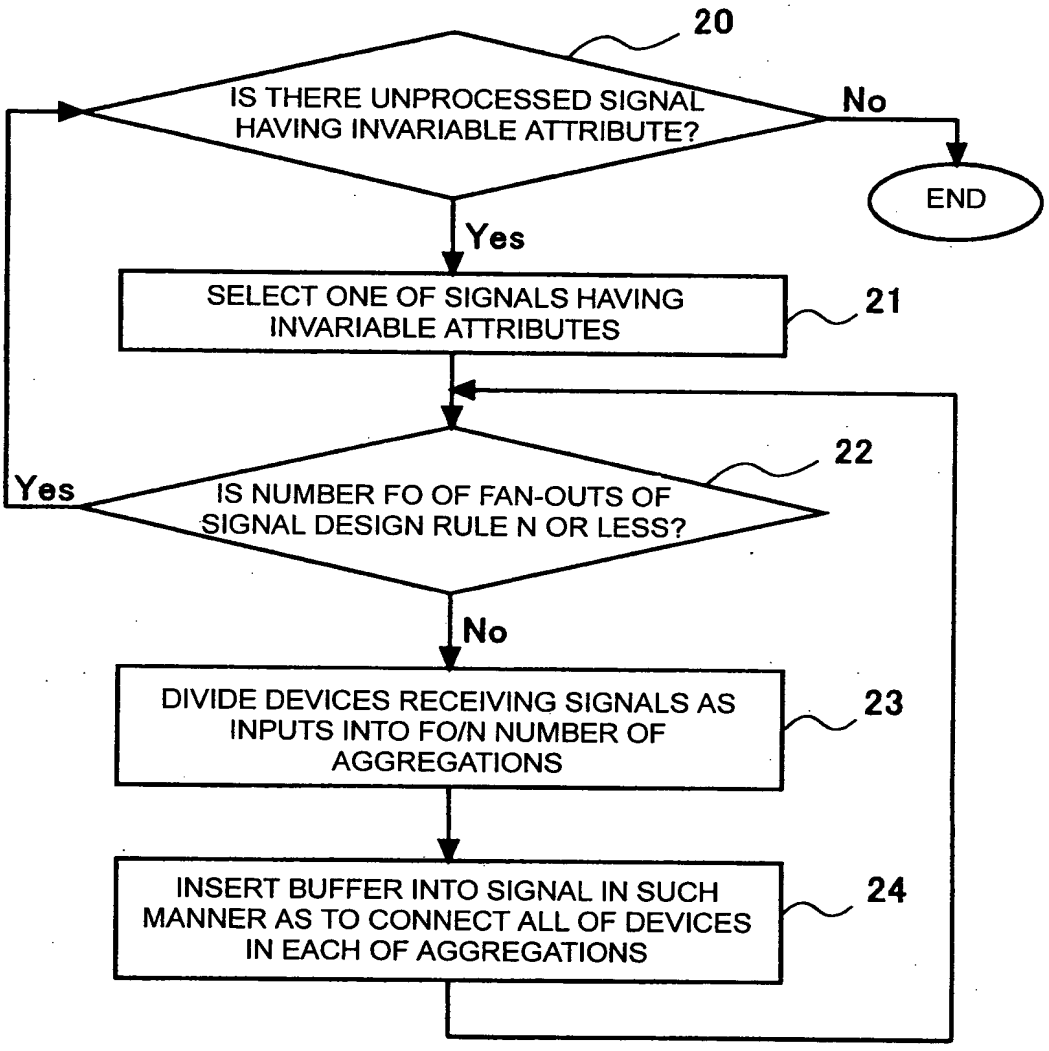
20
IS THERE UNPROCESSED SIGNAL HAVING INVARIABLE ATTRIBUTE?
No
END
Yes
SELECT ONE OF SIGNALS HAVING INVARIABLE ATTRIBUTES
21
22
Yes
IS NUMBER FO OF FAN-OUTS OF SIGNAL DESIGN RULE N OR LESS?
No
DIVIDE DEVICES RECEIVING SIGNALS AS INPUTS INTO FO/N NUMBER OF AGGREGATIONS
23
INSERT BUFFER INTO SIGNAL IN SUCH MANNER AS TO CONNECT ALL OF DEVICES IN EACH OF AGGREGATIONS
24

FIG. 4A

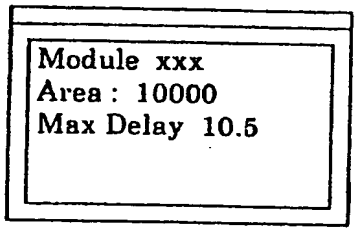

FIG. 4B

from	to	delay
block1/rega	block2/regb	9.4
block2/regb	block2/regc	5.6
block2/regc	block3/regd	10.4

FIG. 4C

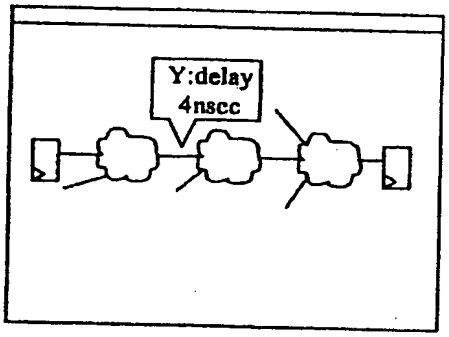

FIG. 4D

```
always @(A or B or C or D) begin
   if (D==1'b0) begin
      Y=A + B;
   end
   else begin
      Y=A + C;
   end
end
```

FIG. 5A

```
always @(A or B or C or D) begin
   if (D==1'b0) begin
     Y=A + B;
   end
   else begin
     Y=A + C;
   end
end
```

FIG. 5B

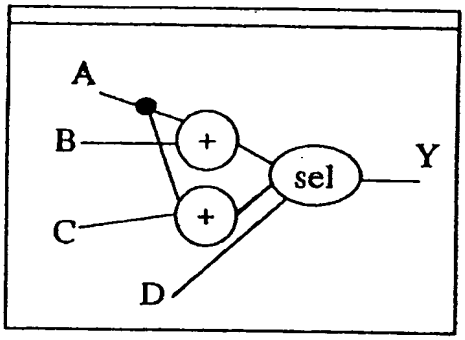

FIG. 5C

Signal	arrival
A	3.5
B	2.6
C	2.8
D	2.0
Y	9.6

FIG. 5D

Signal	arrival
A	3.5
B	2.6
C	2.8
D	4.0
Y	9.6

FIG. 6A

```
always @(A or B or C or D) begin
   if (D==1'b0) begin
     Z=B;
   end
   else begin
     Z=C;
   end
   Y=A+Z;
end
```

FIG. 6B

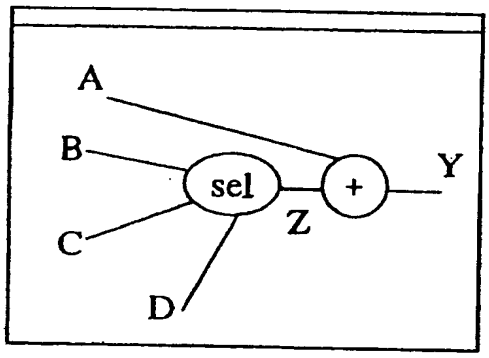

FIG. 6C

Signal	arrival
A	3.5
B	2.6
C	2.8
D	2.0
Y	8.9

FIG. 6D

Signal	arrival
A	3.5
B	2.6
C	2.8
D	4.0
Y	10.1

FIG. 7

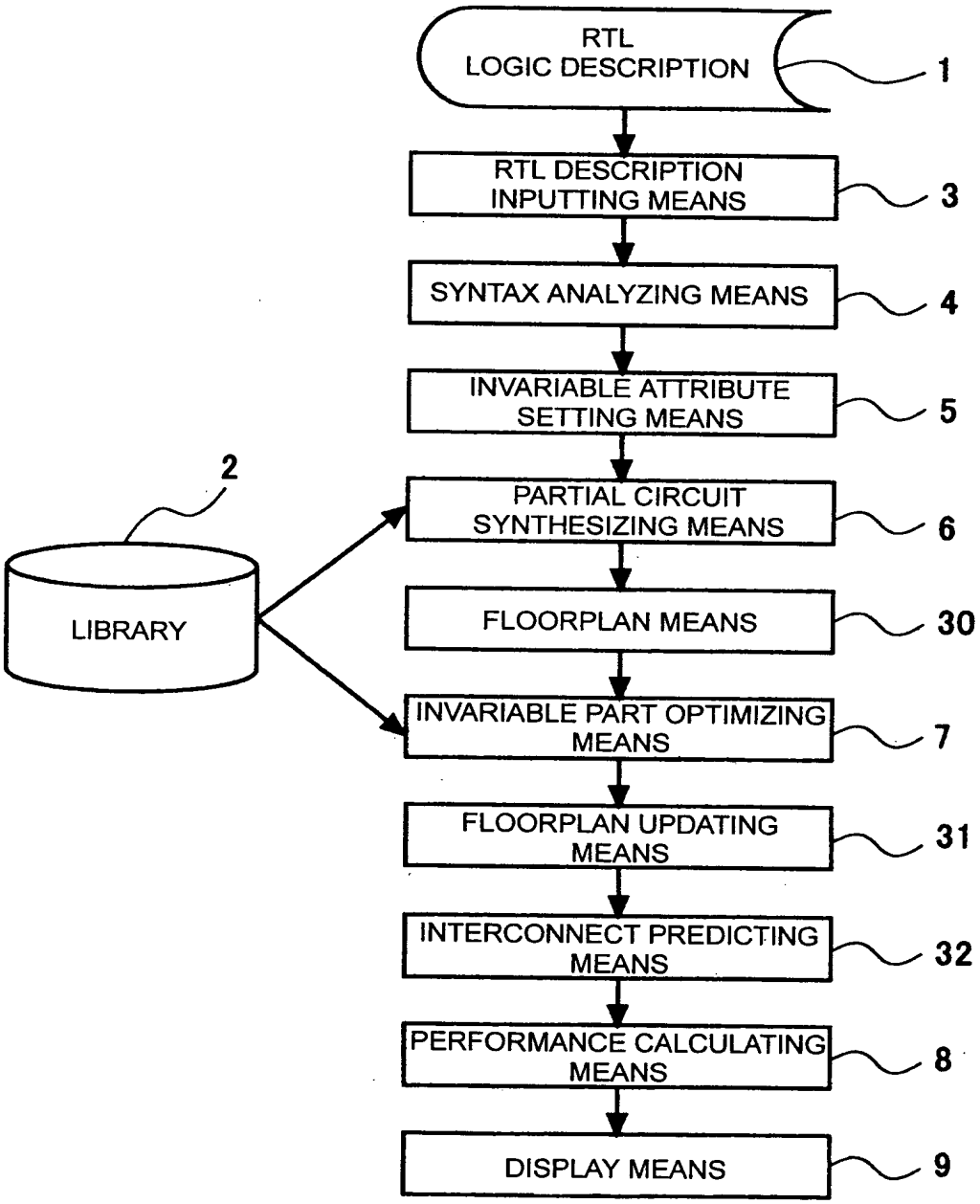
RTL
LOGIC DESCRIPTION
1
RTL DESCRIPTION
INPUTTING MEANS
3
SYNTAX ANALYZING MEANS
4
INVARIABLE ATTRIBUTE
SETTING MEANS
5
2
PARTIAL CIRCUIT
SYNTHESIZING MEANS
6
LIBRARY
FLOORPLAN MEANS
30
INVARIABLE PART OPTIMIZING
MEANS
7
FLOORPLAN UPDATING
MEANS
31
INTERCONNECT PREDICTING
MEANS
32
PERFORMANCE CALCULATING
MEANS
8
DISPLAY MEANS
9

FIG. 8

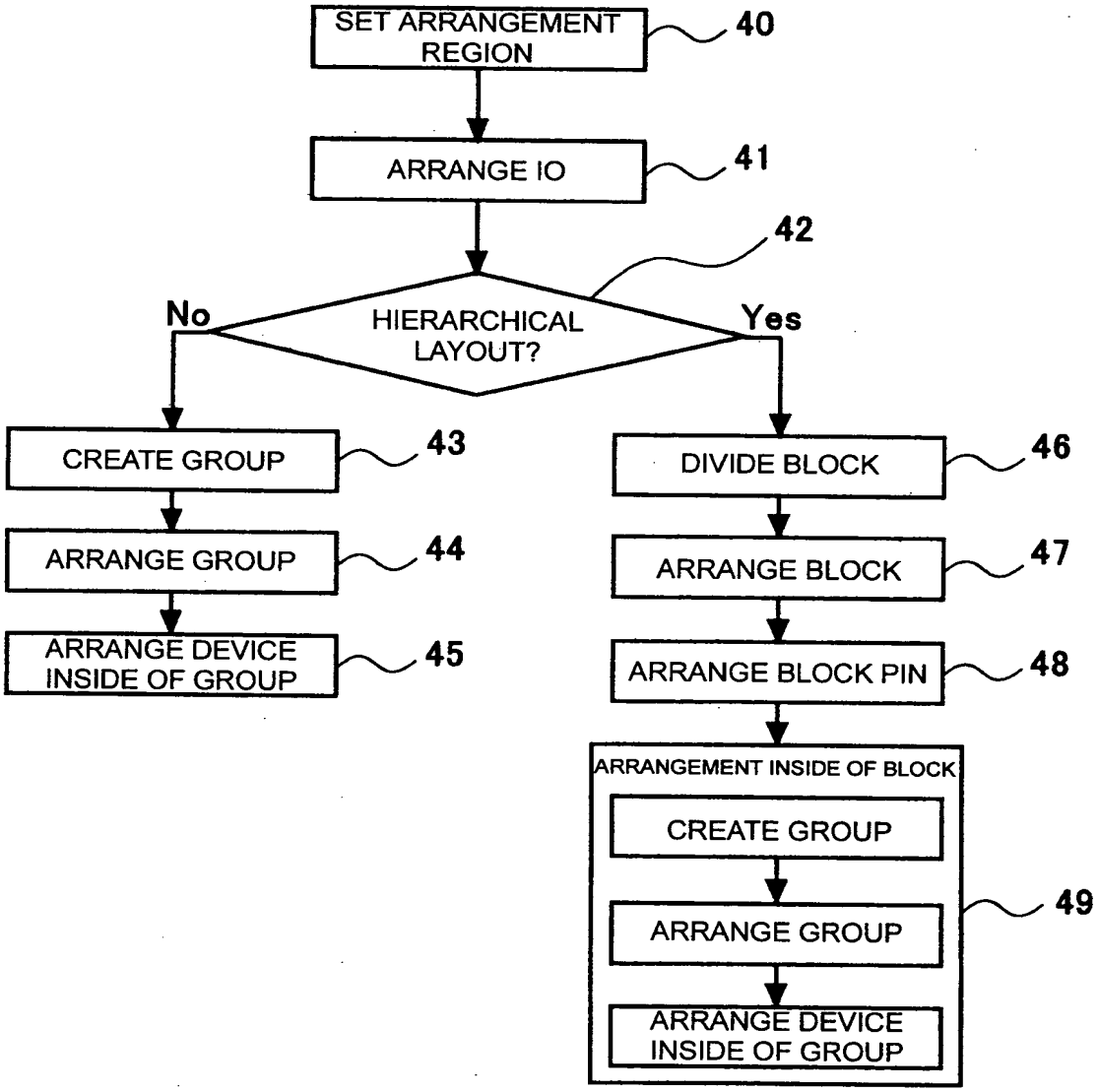
SET ARRANGEMENT REGION
40
ARRANGE IO
41
42
HIERARCHICAL LAYOUT?
No
Yes
CREATE GROUP
43
ARRANGE GROUP
44
ARRANGE DEVICE INSIDE OF GROUP
45
DIVIDE BLOCK
46
ARRANGE BLOCK
47
ARRANGE BLOCK PIN
48
ARRANGEMENT INSIDE OF BLOCK
CREATE GROUP
ARRANGE GROUP
ARRANGE DEVICE INSIDE OF GROUP
49

FIG. 9

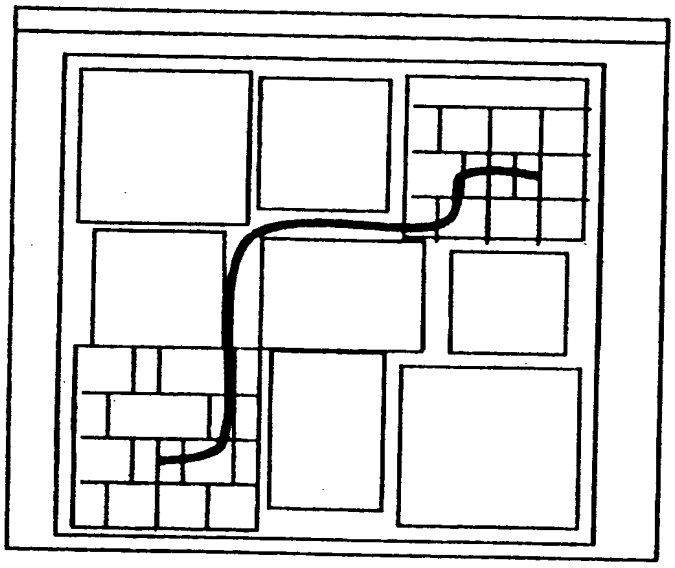

FIG. 10

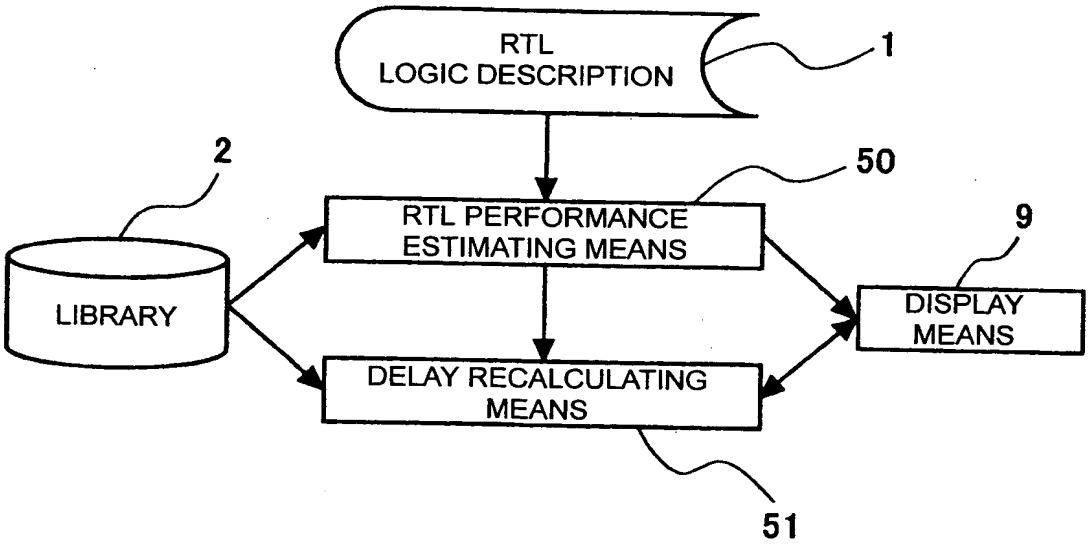
RTL
LOGIC DESCRIPTION
1
2
50
RTL PERFORMANCE
ESTIMATING MEANS
9
LIBRARY
DISPLAY
MEANS
DELAY RECALCULATING
MEANS
51

FIG. 11A

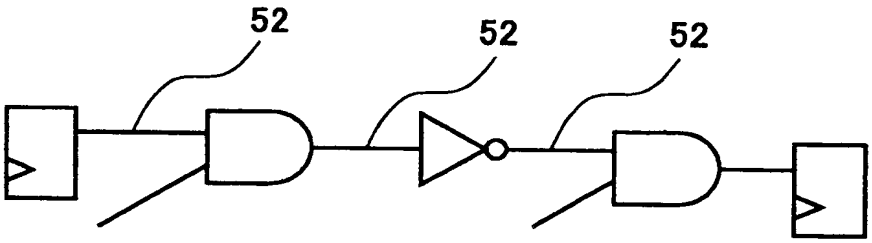

FIG. 11B